What is claimed is:

Sub B1

1. A method of manufacturing a power transistor circuit, comprising:

securing a die to a substrate, the die comprising a transistor having an input terminal;

measuring a performance characteristic of the transistor;

using one or more wires to electrically couple the transistor input terminal to an input matching element, an input signal lead, or both; and

setting the impedance of the one or more wires based at least in part on the measured transistor performance characteristic.

2. The method of claim 1, wherein the performance characteristic is defined, at least in part, by one or more of input capacitance, impedance, gain flatness, and signal phase shift.

3. The method of claim 1, wherein the impedance of the one or more wires is set by selecting a number of wires used to make at least one electrical connection of the transistor circuit.

4. The method of claim 1, wherein the impedance of the one or more wires is set by selecting a length of at least one wire used to make at least one electrical connection of the transistor circuit.

5. A method of manufacturing a power transistor circuit, comprising:

securing a die to a substrate, the die comprising a transistor having an output terminal;

measuring a performance characteristic of the transistor;

using one or more wires to electrically couple the transistor output terminal to an output matching element, an output signal lead, or both; and

setting the impedance of the one or more wires based at least in part on the measured transistor performance characteristic.

6. The method of claim 5, wherein the performance characteristic is defined, at least in part, by one or more of output capacitance impedance, gain flatness, and signal phase shift.

7. The method of claim 5, wherein the impedance of the one or more wires is set by selecting a number of wires used to make at least one electrical connection of the transistor circuit.

8. The method of claim 5, wherein the impedance of the one or more wires is set by selecting a length of at least one wire used to make at least one electrical connection of the transistor circuit.

9. A power transistor circuit, comprising:

a substrate;

a die secured to the substrate, the die comprising a transistor having an input terminal;

one or both of an input lead and an input matching element secured to the substrate; and

one or more wires electrically coupling the transistor input terminal to the one or both of the input matching element and input signal lead, wherein the impedance of the one or more wires is based at least in part on a performance characteristic of the transistor measured after the die is secured to the substrate.

10. The circuit of claim 9, wherein the performance characteristic is defined, at least in part, by one or more of input capacitance, impedance, gain flatness, and signal phase shift.

11. The circuit of claim 9, wherein the impedance of the one or more wires is determined by selecting a number of wires used to make at least one electrical connection of the transistor circuit.

12. The circuit of claim 9, wherein the impedance of the one or more wires is determined by selecting a length of at least one wire used to make at least one electrical connection of the transistor circuit.

13. A power transistor circuit, comprising:

a substrate;

a die secured to the substrate, the die comprising a transistor having an output terminal;

one or both of an output lead and an output matching element secured to the substrate; and

one or more wires electrically coupling the transistor output terminal to the one or both of the output matching element and output signal lead, wherein the impedance of the one or more wires is based at least in part on a performance characteristic of the transistor measured after the die is secured to the substrate.

14. The circuit of claim 13, wherein the performance characteristic is defined, at least in part, by one or more of output capacitance, impedance, gain flatness, and signal phase shift.

15. The circuit of claim 13, wherein the impedance of the one or more wires is determined by selecting a number of wires used to make at least one electrical connection of the transistor circuit.

16. The circuit of claim 13, wherein the impedance of the one or more wires is determined by selecting a length of at least one wire used to make at least one electrical connection of the transistor circuit.